formed on the substrate and the gate layer, wherein the first insulator layer has a flat part and two vertical walls, the flat part being formed between the two vertical walls; a semiconductor layer formed on the first insulator layer, wherein the semiconductor layer has two channels formed on the two vertical walls, and a first doped area and a second doped area formed to connect with the ends of the two channels respectively, and an intrinsic area formed on the flat part between the first doped area and the second doped area; a second insulator layer formed and covering over the two channels; and a metal layer formed on the semiconductor layer separately.

The process of the present invention successfully decreases the fabrication cost by simplifying the conventional CMOS process. Furthermore, leakage current is also reduced in the above CMOS with a dual gate and offset structure. Moreover, the double vertical channel (DVC) structure of the above CMOS side steps the photolithography limitation because the deep-submicrometer channel length is determined by the thickness of gate, thereby decreasing the channel length substantially.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be more fully understood by reading the subsequent detailed description in conjunction with the examples and references made to the accompanying drawings, wherein: (6a - 6b)

Figs. 1 to 6 are sectional views showing an embodiment of the CMOS process for double vertical channel thin film transistor according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Embodiment 1

As shown in Fig. 1, a gate layer **20** is deposited on a substrate **10**. The gate layer **20**, is preferably deposited by APCVD, LPCVD, PECVD, sputtering system, or e-gun evaporation, and is preferably composed of doped polysilicon, doped amorphous silicon, transition metals, metal silicide, polycide of metal, aluminum, aluminum alloy, or copper.

As shown in Fig. 2, a gate insulator layer **30** is deposited on the substrate **10** and the gate layer **20**. The gate insulator layer **30**, is preferably deposited by APCVD, LPCVD, PECVD, sputtering system, or e-gun evaporation, and is preferably composed of nitride, oxide, or oxynitride.

As shown in Fig. 3, a semiconductor layer **40** is deposited on the gate insulator layer **30**. The semiconductor layer **40**, is preferably deposited by APCVD, LPCVD, PECVD, sputtering system, or e-gun evaporation, and is preferably composed of single crystal silicon, polysilicon, amorphous silicon, or silicon-~~germaium~~. germanium

As shown in Fig. 4, a mask **50** is deposited on the surface of I area of the semiconductor layer **40**, and N^+ ions are implanted to the other surface of the semiconductor layer **40** to define a N^+ doped area **42** and a channel **46**. Then, the mask **50** is removed. Furthermore, as shown in Fig. 5, a mask **52** is deposited on the surface of II area of the semiconductor layer **40**, and P^+ ions are implanted to the other surface of the semiconductor layer **40** to define a P^+ doped area **44** and a channel **46** of the II area and an intrinsic area **54** of the III area. Then, the mask **52** is removed. In this case, the two channels **46** are called double vertical channel (DVC). The DVC structure side steps the conventional photolithography limitation because the